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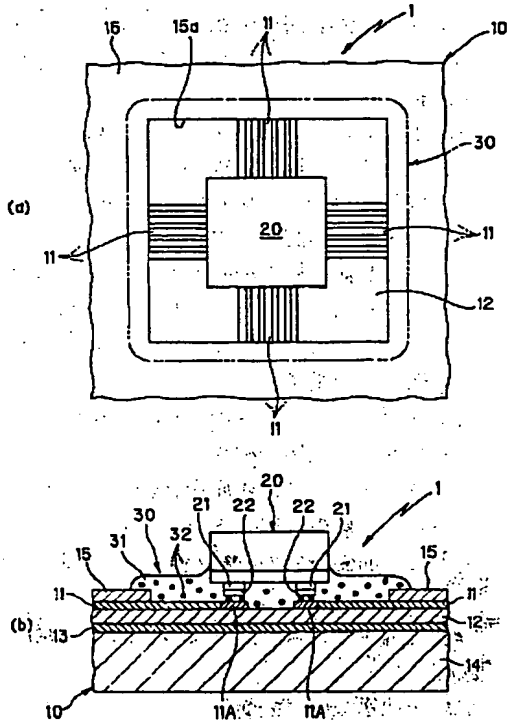
(54)【発明の名称】　配線基板および電子ユニットおよび電子部品実装方法

(57)【要約】
【課題】　本発明の課題は、配線基板と電子部品との接合性の低下を未然に防止することの可能な、配線基板および電子ユニットおよび電子部品実装方法を提供することにある。
【解決手段】　本発明の配線基板１０は、表層の配線パターン１１の直下における絶縁層１２を、ガラスクロスに樹脂を含浸させて形成している。また、本発明の電子ユニット１は、表層の配線パターン１１の直下における絶縁層１２を、ガラスクロスに樹脂を含浸させて形成した配線基板１０に、異方性導電接合材料３０を介してベアＩＣチップ２０を実装している。また、本発明の電子部品実装方法は、配線基板１０の実装面にフィルム状の異方性導電接合材料３０を載置する工程と、フィルム状の異方性導電接合材料３０をヒートツール４０の柔軟性および耐熱性を備えたパッド４１により加圧および加熱して配線基板１０の実装面に仮付けする工程とを含んでいる。



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【特許請求の範囲】

【請求項１】　絶縁層を挟んで積層された配線パターンを具備し、前記配線パターンと前記絶縁層とを順次積層して製造されるビルドアップ型の配線基板であって、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成したことを特徴とする配線基板。

【請求項２】　絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成し、前記配線パターンと前記絶縁層とを順次積層して製造されるビルドアップ型の配線基板に、異方性導電接合材料を介して電子部品を実装して成ることを特徴とする電子ユニット。

【請求項３】　絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成し、前記配線パターンと前記絶縁層とを順次積層して製造されるビルドアップ型の配線基板に、異方性導電接合材料を介して電子部品を実装する電子部品実装方法であって、
前記配線基板の実装面にフィルム状の異方性導電接合材料を載置する工程と、
前記フィルム状の異方性導電接合材料を、ヒートツールの柔軟性および耐熱性を備えたパッドにより加圧および加熱して、前記配線基板の実装面に仮付けする工程と、
を含んで成ることを特徴とする電子部品実装方法。

【請求項４】　絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、前記表層の配線パターンの表面を覆うソルダーレジストに、前記表層の配線パターンに実装される電子部品の外形よりも大きい開口を形成したことを特徴とする配線基板。

【請求項５】　絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、前記表層の配線パターンの表面を覆うソルダーレジストに、前記表層の配線パターンに実装される電子部品の外形よりも大きい開口を形成して成る配線基板に、異方性導電接合材料を介して電子部品を実装して成ることを特徴とする電子ユニット。

【請求項６】　絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、前記表層の配線パターンの表面を覆うソルダーレジストに、前記表層の配線パターンに実装される電子部品の外形よりも大きい開口を形成して成る配線基板に、異方性導電接合材料を介して電子部品を実装する電子部品実装方法であって、
前記配線基板の実装面にフィルム状の異方性導電接合材料を載置する工程と、

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前記フィルム状の異方性導電接合材料を、ヒートツールの柔軟性および耐熱性を備えたパッドにより加圧および加熱して、前記配線基板の実装面に仮付けする工程と、
を含んで成ることを特徴とする電子部品実装方法。

【請求項７】　絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、前記表層の配線パターンにおける電極を、先端部のコーナーを切欠いた形状とすることを特徴とする配線基板。

【請求項８】　絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、前記表層の配線パターンにおける電極を、先端部のコーナーを切欠いた形状として成る配線基板に、異方性導電接合材料を介して電子部品を実装して成ることを特徴とする電子ユニット。

【請求項９】　絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、前記表層の配線パターンにおける電極を、先端部のコーナーを切欠いた形状として成る配線基板に、異方性導電接合材料を介して電子部品を実装する電子部品実装方法であって、
前記配線基板の実装面にフィルム状の異方性導電接合材料を載置する工程と、
前記フィルム状の異方性導電接合材料を、ヒートツールの柔軟性および耐熱性を備えたパッドにより加圧および加熱して、前記配線基板の実装面に仮付けする工程と、
を含んで成ることを特徴とする電子部品実装方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、絶縁層を挟んで積層された配線パターンを具備する配線基板と、この配線基板に電子部品を実装して成る電子ユニットと、この電子ユニットを製造する際の電子部品実装方法に関するものである。

【０００２】

【従来の技術】電子部品である半導体装置を、配線基板(プリント配線板)に実装する方法の１つとして、異方性導電接合材料を用いたフリップチップ実装方法（フリップチップボンディング法）がある。

【０００３】図９は、フリップチップ実装方法を用いて製造された電子ユニットＡであり、配線基板Ｂに電子部品であるベアＩＣチップＣが異方性導電接合材料Ｄを介して実装されている。

【０００４】図１０に示す如く、配線基板Ｂは配線パターンと絶縁層とが交互に積層されており、実装面(図中上面)には導電材料から成る配線パターンＢ１，Ｂ１…

が形成され、各々の配線パターンＢ１の先端には、金メッキにより各々電極Ｂ１ａが形成されている。

【０００５】表層の配線パターンＢ１の直下には、絶縁性樹脂から形成された絶縁層Ｂ２が形成され、この絶縁層Ｂ２の直下には配線パターンＢ３が形成され、さらに配線パターンＢ３の直下には絶縁層Ｂ４が形成されている。

【０００６】また、図１０に示す如く、表層の配線パターンＢ１，Ｂ１…は、各電極Ｂ１ａの部分を除いて、表面をソルダーレジストＢｒにより覆われている。

【０００７】一方、図９に示す如く、電子部品であるベアＩＣチップＣは、その実装面（図中底面）に、配線基板Ｂの電極Ｂ１ａ，Ｂ１ａ…と対応する電極Ｃａ，Ｃａ…が設けられ、各電極Ｃａ，Ｃａ…の表面には各々バンプＣｂが形成されている。

【０００８】上述した電子ユニットＡを製造するには、先ず、図１１（ａ）に示す如く、配線基板Ｂの実装面に、フィルム状の異方性導電接合材料（異方性導電フィルム）Ｄを載置する。なお、異方性導電接合材料Ｄは、周知の如く絶縁性樹脂Ｄａに導電粒子Ｄｂ，Ｄｂ…を混在させることにより形成されている。

【０００９】次いで、図１１（ｂ）に示す如く、異方性導電接合材料Ｄを、ヒートツールＨによって加熱かつ上方から加圧して、配線基板Ｂに異方性導電接合材料Ｄを仮接着する。なお、ヒートツールＨのパッドＨｐは、ステンレス等の金属材料から形成されており、内部には図示していない加熱用ヒータが設けられている。

【００１０】次いで、配線基板Ｂに仮接着された異方性導電接合材料Ｄに、図示していないベアＩＣチップＣを載置したのち、ヒートツールＨによって、ベアＩＣチップＣを加圧し、かつ異方性導電接合材料Ｄを加熱することで、ベアＩＣチップＣを配線基板Ｂに本接着する。

【００１１】かくすることで、配線基板Ｂとベアチップ ＩＣチップＣとが、異方性導電接合材料Ｄの絶縁性樹脂Ｄａにより接合され、配線基板Ｂの各電極Ｂ１ａとベアＩＣチップＣの各電極Ｃａ（バンプＣｂ）との間に、異方性導電接合材料Ｄの導電粒子Ｄｂ，Ｄｂ…が介在することで電気的に接続される。

【００１２】

【発明が解決しようとする課題】ところで、従来の電子ユニットＡを構成する配線基板Ｂは、表層の配線パターンＢ１，Ｂ１…の直下に位置する絶縁層Ｂ２が、絶縁性樹脂から形成されているため、配線基板Ｂに異方性導電接合材料Ｄを仮接着する際の加圧および加熱、さらには配線基板Ｂにベアチップ ＩＣチップＣを本接着する際の加圧および加熱の影響で、上記絶縁層Ｂ２が変形することにより、表層の配線パターンＢ１および電極Ｂ１ａが変形してしまう。

【００１３】これにより、配線基板Ｂに対するベアＩＣチップＣの接合性、すなわち異方性導電接合材料Ｄの絶縁性樹脂Ｄａによる機械的な接合性、および異方性導電接合材料Ｄの導電粒子Ｄｂによる電気的な接合性が低下する不都合があった。

【００１４】本発明は、上記実状に鑑みて、表層の配線パターン直下の絶縁層の変形に起因する、配線基板と電子部品との接合性の低下を未然に防止することの可能な、配線基板および電子ユニットおよび電子部品実装方法の提供を目的とする。

【００１５】一方、従来の電子ユニットＡを構成する配線基板Ｂは、図９および図１０に示す如く、ソルダーレジストＢｒが電極Ｂ１ａ，Ｂ１ａ…のみを露呈させる態様で表層の配線パターンＢ１，Ｂ１…を覆っているため、配線基板Ｂにベアチップ ＩＣチップＣを実装した際、ベアＩＣチップＣの縁部底面がソルダーレジストＢｒに乗り上げてしまう虞れがある。

【００１６】これにより、配線基板Ｂにおける各電極Ｂ１ａと、ベアＩＣチップＣにおける各電極Ｃａ（バンプＣｂ）との、異方性導電接合材料Ｄの導電粒子Ｄｂを介しての接続が不完全なものとなり、配線基板Ｂに対するベアＩＣチップＣの接合性が低下する不都合があった。

【００１７】本発明は、上記実状に鑑みて、ソルダーレジストの形状に起因する、配線基板と電子部品との接合性の低下を未然に防止することの可能な、配線基板および電子ユニットおよび電子部品実装方法の提供を目的とする。

【００１８】一方、従来の電子ユニットＡを構成する配線基板Ｂでは、図１０に示す如く、各配線パターンＢ１における電極Ｂ１ａの平面形状が矩形状を呈しており、配線基板Ｂとベアチップ ＩＣチップＣとの電気的な接続効率を向上させるには、接触面積を増大させるべく電極Ｂ１ａの先端を延長させることが望ましい。

【００１９】しかしながら、コーナー部分において隣接する電極同士が干渉してショートする虞れがあるため、配線パターンＢ１の電極Ｂ１ａを大型化することが難しく、もって電気的な接続性の低下を余儀なくされていた。

【００２０】また、各配線パターンＢ１における電極Ｂ１ａの先端部が角張っているため、配線基板Ｂにベアチップ ＩＣチップＣを本接着する工程で、溶融した異方性導電接合材料Ｄの絶縁性樹脂Ｄａが、隣接する配線パターンＢ１，Ｂ１の間に先端側から流入し難く、絶縁性樹脂Ｄａ中にボイドを生じる虞れがあり、もって機械的な接続性の低下を招いてしまう不都合があった。

【００２１】本発明は、上記実状に鑑みて、配線パターンにおける電極の形状に起因する、配線基板と電子部品との接合性の低下を未然に防止することの可能な、配線基板および電子ユニットおよび電子部品実装方法の提供を目的とする。

【００２２】一方、従来の電子ユニットＡを製造する際、配線基板Ｂに異方性導電接合材料Ｄを仮接着する工

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程で使用されるヒートツールHは、上述した如くパッドHpがステンレス等の硬い金属材料から形成されているため、図11(b)に示す如く、異方性導電接合材料Dは、各配線パターンB1(電極B1a)やソルダーレジストBrの積層された配線基板Bの実装面に追従しない。

【0023】このため、配線基板Bに対する異方性導電接合材料Dの確実な仮接着が行われず、後の工程における配線基板BとベアICチップCとの本接着が不完全なものとなり、配線基板Bに対するベアICチップCの接合性が低下してしまう不都合があった。

【0024】本発明は、上記実状に鑑みて、ヒートツールの材質に起因する、配線基板と電子部品との接合性の低下を未然に防止することの可能な、電子部品実装方法の提供を目的とする。

【0025】

【課題を解決するための手段】上記目的を達成するべく、請求項1に関わる配線基板では、絶縁層を挟んで積層された配線パターンを具備し、この配線パターンと絶縁層とを順次積層して製造されるビルドアップ型の配線基板において、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成している。

【0026】また、請求項2に関わる電子ユニットでは、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成し、この配線パターンと絶縁層とを順次積層して製造されるビルドアップ型の配線基板に、異方性導電接合材料を介して電子部品を実装している。

【0027】また、請求項3に関わる電子部品実装方法では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成し、この配線パターンと絶縁層とを順次積層して製造されるビルドアップ型の配線基板に、異方性導電接合材料を介して電子部品を実装する電子部品実装方法において、配線基板の実装面にフィルム状の異方性導電接合材料を載置する工程と、フィルム状の異方性導電接合材料をヒートツールの柔軟性および耐熱性を備えたパッドにより加圧および加熱して配線基板の実装面に仮付けする工程とを含んでいる。

【0028】また、請求項4に関わる配線基板では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンの表面を覆うソルダーレジストに、表層の配線パターンに実装される電子部品の外形よりも大きい開口を形成している。

【0029】また、請求項5に関わる電子ユニットでは、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の

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配線パターンの表面を覆うソルダーレジストに、表層の配線パターンに実装される電子部品の外形よりも大きい開口を形成して成る配線基板に、異方性導電接合材料を介して電子部品を実装している。

【0030】また、請求項6に関わる電子部品実装方法では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンの表面を覆うソルダーレジストに、表層の配線パターンに実装される電子部品の外形よりも大きい開口を形成して成る配線基板に、異方性導電接合材料を介して電子部品を実装する電子部品実装方法において、配線基板の実装面にフィルム状の異方性導電接合材料を載置する工程と、フィルム状の異方性導電接合材料をヒートツールの柔軟性および耐熱性を備えたパッドにより加圧および加熱して配線基板の実装面に仮付けする工程とを含んでいる。

【0031】また、請求項7に関わる配線基板では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンにおける電極を、先端部のコーナーを切欠いた形状としている。

【0032】また、請求項8に関わる電子ユニットでは、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンにおける電極を、先端部のコーナーを切欠いた形状として成る配線基板に、異方性導電接合材料を介して電子部品を実装している。

【0033】また、請求項9に関わる電子部品実装方法では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンにおける電極を、先端部のコーナーを切欠いた形状として成る配線基板に、異方性導電接合材料を介して電子部品を実装する電子部品実装方法であって、配線基板の実装面にフィルム状の異方性導電接合材料を載置する工程と、フィルム状の異方性導電接合材料をヒートツールの柔軟性および耐熱性を備えたパッドにより加圧および加熱して配線基板の実装面に仮付けする工程とを含んでいる。

【0034】

【発明の実施の形態】以下、一実施例を示す図面に基づいて、本発明を詳細に説明する。図1(a),(b)は、フリップチップ実装方法を用いて製造された、本発明に関わる電子ユニット1を示しており、この電子ユニット1は配線基板10と、電子部品としてのベアICチップ20とを備え、異方性導電接合材料30を用いて配線基板10にベアICチップ20を実装して構成されている。

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【００３５】また、前記電子ユニット１は、後に詳述する如く、配線基板１０に異方性導電接合材料３０を載置する工程と、同じく異方性導電接合材料３０を仮接着する工程と、異方性導電接合材料３０にベアＩＣチップ２０を載置する工程と、配線基板１０にベアＩＣチップ２０を本接着する工程とを経て製造される。

【００３６】電子ユニット１を構成する配線基板１０は、後述する複数の配線パターンおよび絶縁層を順次積層して製造される、いわゆるビルドアップ型の配線基板（ビルドアップ基板）であり、図１および図２に示す如く、配線基板１０の実装面（図中上面）には、表層の配線パターン１１，１１…が形成されている。

【００３７】前記表層の配線パターン１１，１１…の直下には、絶縁層１２が形成されており、この絶縁層１２は、ガラスクロスに樹脂を含浸させることにより形成されている。また、絶縁層１２の直下には配線パターン１３が形成され、さらに配線パターン１３の直下には絶縁層１４が形成されている。

【００３８】配線基板１０における表層の配線パターン１１，１１…は、導電材料から形成されており、各々の配線パターン１１，１１…の先端には、金メッキが施されることによって電極１１Ａ，１１Ａ…が形成されている。また、各々の配線パターン１１における電極１１Ａは、図３に示す如く、先端部のコーナーを切欠いた形状を呈している。

【００３９】図１および図２に示す如く、配線基板１０における表層の配線パターン１１，１１…の表面は、ソルダーレジスト１５によって覆われており、このソルダーレジスト１５には、前記配線パターン１１，１１…の電極１１Ａ，１１Ａ…を露呈させる開口１５ａが、配線基板１０に実装されるベアＩＣチップ２０の外形よりも遙かに大きく形成されている。

【００４０】なお、上述した構成の配線基板１０は、ビルドアップ型の配線基板に限定されるものではなく、絶縁層１４に配線パターン１３形成した基板ユニットと、絶縁層１２に配線パターン１１を形成した基板ユニットとを、互いに重ねて熱圧着することで製造される極く通常の配線基板であっても良い。

【００４１】一方、電子部品としてのベアＩＣチップ２０は、図１（ｂ）に示す如く、配線基板１０と対向する実装面（図中底面）に、Ａｌ（アルミニウム）等の導電材料から成る電極２１，２１…が形成されている。

【００４２】これら電極２１，２１…は、配線基板１０における各電極１１Ａ，１１Ａ…と対応して配置されており、ベアＩＣチップ２０の電極２１，２１…の表面には、Ａｕ（金）あるいはＳｎ－Ｐｂ（錫－鉛）合金等によってバンプ２２，２２…が形成されている。

【００４３】以下では、上述した構成の電子ユニット１を製造する方法、言い換えれば配線基板１０に対するベアＩＣチップ２０の実装方法を説明する。

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【００４４】先ず、図５に示す如く、配線基板１０の実装面に、フィルム状の異方性導電接合材料（異方性導電フィルム）３０を載置する。ここで、異方性導電接合材料３０は、絶縁性樹脂３１に導電粒子３２，３２…を混在させ、フィルム状に形成したものであり、図５に示す如く、ソルダーレジスト１５の開口１５ａを十分に覆う大きさを有している。

【００４５】次いで、図６に示す如く、フィルム状の異方性導電接合材料３０を、ヒートツール４０によって加熱かつ上方から加圧して、配線基板１０に異方性導電接合材料３０を仮接着する。

【００４６】ここで、ヒートツール４０は、図示していない加熱用ヒータを内蔵したパッド４１を備えており、このパッド４１は、例えばシリコン系耐熱樹脂やテフロン系耐熱樹脂等、柔軟性と耐熱性とを具備した材料によって構成されている。

【００４７】このため、パッド４１によって異方性導電接合材料３０を加圧した際、パッド４１が変形することにより、異方性導電接合材料３０の全体が配線基板１０の実装面に密着し、配線基板１０に対して異方性導電接合材料３０が確実に仮接着されることとなる。

【００４８】次いで、図７に示す如く、仮接着された異方性導電接合材料３０に、ベアＩＣチップ２０を載置する。このとき、ベアＩＣチップ２０の各電極２１（バンプ２２）を、配線基板１０の各電極１１Ａに対応させる位置態様で、異方性導電接合材料３０にベアＩＣチップ２０を載置する。

【００４９】この後、図８に示す如く、先に異方性導電接合材料３０を仮接着したと同一のヒートツール４０を用いて、ベアＩＣチップ２０を加圧するとともに、異方性導電接合材料３０を加熱することにより、ベアＩＣチップ２０を配線基板１０に本接着する。

【００５０】かくして、配線基板１０とベアＩＣチップ２０とが、溶融したのち硬化した異方性導電接合材料３０の絶縁性樹脂３１によって接合され、配線基板１０の各電極１１Ａとベアチップ２０の各電極２１（バンプ２２）との間に、異方性導電接合材料３０の導電粒子３２，３２…が介在することで電気的に接続される。

【００５１】上述した如く、配線基板１０にベアＩＣチップ２０を実装する場合、配線基板１０に異方性導電接合材料３０を仮接着する際、および配線基板１０にベアＩＣチップ２０を本接着する際には、配線基板１０に対して加圧および加熱が作用することとなる。

【００５２】これに対して、配線基板１０における表層の配線パターン１１の直下に位置する絶縁層１２は、ガラスクロスに樹脂を含浸させて形成されているため、従来の絶縁性樹脂から形成された絶縁層に比べて剛性が向上しており、配線基板１０への加熱および加圧に対する絶縁層１２の変形、延いては配線パターン１１（電極１１Ａ）の変形が可及的に抑えられる。

【００５３】これにより、配線基板１０に対するベアＩＣチップ２０の接合性、すなわち異方性導電接合材料３０の絶縁性樹脂３１による機械的な接合性、および異方性導電接合材料３０の導電粒子３２による電気的な接合性の低下を未然に防止することができる。

【００５４】また、上述した如く、配線基板１０にベアＩＣチップ２０を実装する場合、従来ではベアＩＣチップの縁部底面がソルダーレジストに乗り上げてしまう虞れがあったのに対し、配線基板１０におけるソルダーレジスト１５には、ベアＩＣチップ２０の外形よりも大きい開口１５ａが形成されているため、ベアＩＣチップ２０がソルダーレジスト１５に乗り上げてしまうことはない。

【００５５】このため、配線基板１０の各電極１１Ａと、ベアＩＣチップ２０の各電極２１(バンプ２２)とが、異方性導電接合材料３０の導電粒子３２を介して確実に接続され、もって配線基板１０に対するベアＩＣチップ２０の接合性の低下を未然に防止することが可能となる。

【００５６】さらに、ソルダーレジスト１５の開口１５ａは、電子ユニット１が完成した状態において、図１に示す如く異方性導電接合材料３０によって覆われるため、表層の配線パターン１１が大気中に露出することなく封止され、酸化や外力から保護されるとともに、別途の絶縁性樹脂を用いて封止するものでないため、電子ユニット１の製造工程を徒らに繁雑化することもない。

【００５７】また、上述した如く、配線基板１０における表層の配線パターン１１，１１…の電極１１Ａ，１１Ａ…は、図３に示す如く、先端部のコーナーを切欠いた形状を呈しており、特にコーナー部分において隣接する電極１１Ａ，１１Ａは、対向するコーナーを切欠いた形状を呈しているので、互いのショートを防止しつつ各電極１１Ａの大型化を達成している。

【００５８】さらに、上述したコーナー部分以外の電極１１Ａ，１１Ａ…は、先端部における左右の両コーナーを切欠いた形状を呈しているので、ベアＩＣチップ２０を本接着する際に溶融した異方性導電接合材料３０の絶縁性樹脂３１が、隣接する配線パターン１１，１１の間に先端側から容易に流入することとなる。

【００５９】これにより、配線基板１０とベアＩＣチップ２０との電気的な接続効率、および機械的な接続性が向上し、もって配線基板１０に対するベアＩＣチップ２０の接合性の低下を未然に防止することが可能となる。

【００６０】なお、電極の大型化のみを目的とするならば、図４(ａ)に示す如く、各配線パターン１１の電極１１Ａにおいて、特にコーナー部分において隣接する電極１１Ａ，１１Ａのみコーナーを切欠いた形状とし、その他の電極１１Ａ，１１Ａ…を矩形状とすることも可能であり、また別の態様として、図４(ｂ)に示す如く、各配線パターン１１の電極１１Ａにおいて、コーナー部分で隣接する電極１１Ａ，１１Ａのみ矩形状とし、その他の電極１１Ａ，１１Ａ…をコーナーの切欠かれたた形状としてもよい。

【００６１】また、上述した如く、配線基板１０にベアＩＣチップ２０を実装する場合、従来ではヒートツールのパッドが金属製であったので、異方性導電接合材料が配線基板の実装面に追従せず、配線基板に対して異方性導電接合材料を確実に仮接着できなかったのに対し、ヒートツール４０のパッド４１を柔軟性と耐熱性とを備えた材料から構成したことで、異方性導電接合材料３０の全体を配線基板１０に密着させて確実に仮接着することが可能となった。

【００６２】このため、後の工程における配線基板１０とベアＩＣチップ２０との本接着をも確実に実施することができ、もって配線基板１０に対するベアＩＣチップ２０の接合性の低下を未然に防止することが可能となる。

【００６３】また、配線基板１０にベアＩＣチップ２０を本接着させる際にも、上述したヒートツール４０を用いたことによって、配線基板１０に仮接着された異方性導電接合材料３０に対し、ベアＩＣチップ２０が傾斜して載置された場合でも、ヒートツール４０におけるパッド４１の柔軟性が、上記傾斜を吸収しつつベアＩＣチップ２０を均一に押圧することとなり、もって配線基板１０に対してベアＩＣチップ２０を確実に接続させることが可能となる。

【００６４】なお、上述した実施例においては、配線基板に実装される電子部品としてベアＩＣチップを例示しているが、配線基板に対してフリップチップ実装される電子部品であれば、ベアＩＣチップ以外の様々な電子部品を搭載する配線基板や電子ユニットにおいても、本発明を有効に適用し得ることは言うまでもない。

【００６５】

【発明の効果】以上、詳述した如く、請求項１に関わる配線基板では、絶縁層を挟んで積層された配線パターンを具備し、この配線パターンと絶縁層とを順次積層して製造されるビルドアップ型の配線基板において、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成している。上記構成によれば、表層の配線パターンの直下における絶縁層の剛性が向上するため、配線基板への加熱および加圧に対する前記絶縁層の変形、延いては前記配線パターンの変形が可及的に抑えられ、もって本発明の配線基板によれば、配線基板と電子部品との接合性の低下を未然に防止できる。

【００６６】請求項２に関わる電子ユニットにおいては、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成し、この配線パターンと絶縁層とを順次積層して製造されるビルドアップ型の配線基板に、異方性導電接合材料を介して電子部品を実装し

ている。上記構成によれば、表層の配線パターンの直下における絶縁層の剛性が向上するため、配線基板への加熱および加圧に対する前記絶縁層の変形、延いては前記配線パターンの変形が可及的に抑えられ、もって本発明の電子ユニットによれば配線基板と電子部品との接合性の低下を未然に防止できる。

【００６７】請求項３に関わる電子部品実装方法では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成し、この配線パターンと絶縁層とを順次積層して製造されるビルドアップ型の配線基板に、異方性導電接合材料を介して電子部品を実装する電子部品実装方法において、配線基板の実装面にフィルム状の異方性導電接合材料を載置する工程と、フィルム状の異方性導電接合材料をヒートツールの柔軟性および耐熱性を備えたパッドにより加圧および加熱して配線基板の実装面に仮付けする工程とを含んでいる。上記構成によれば、表層の配線パターンの直下における絶縁層の剛性が向上するため、配線基板への加熱および加圧に対する前記絶縁層の変形、延いては前記配線パターンの変形が可及的に抑えられ、もって本発明の電子部品実装方法によれば、配線基板と電子部品との接合性の低下を未然に防止できる。さらに上記構成では、ヒートツールにおけるパッドの柔軟性により、フィルム状の異方性導電接合材料を、配線基板の実装面に追従させて確実に仮接着でき、もって本発明の電子部品実装方法によれば、配線基板と電子部品との接合性の低下を未然に防止できる。

【００６８】請求項４に関わる配線基板では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンの表面を覆うソルダーレジストに、表層の配線パターンに実装される電子部品の外形よりも大きい開口を形成している。上記構成によれば、表層の配線パターンの直下における絶縁層の剛性が向上するため、配線基板への加熱および加圧に対する前記絶縁層の変形、延いては前記配線パターンの変形が可及的に抑えられ、もって本発明の配線基板によれば、配線基板と電子部品との接合性の低下を未然に防止できる。さらに上記構成によれば、ソルダーレジストの開口が電子部品の外形よりも大きいため、電子部品がソルダーレジストに乗り上げることがなく、もって本発明の配線基板によれば、配線基板と電子部品との接合性の低下を未然に防止することができる。

【００６９】請求項５に関わる電子ユニットにおいては、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンの表面を覆うソルダーレジストに、表層の配線パターンに実装される電子部品の外形よりも大きい開口を形成して成る配線基板に、異方性導電接合材料を介して電子部品を実装している。上記構成によれば、表層の配線パターンの直下における絶縁層の剛性が向上するため、配線基板への加熱および加圧に対する前記絶縁層の変形、延いては前記配線パターンの変形が可及的に抑えられ、もって本発明の電子ユニットによれば配線基板と電子部品との接合性の低下を未然に防止できる。さらに上記構成によれば、ソルダーレジストの開口が電子部品の外形よりも大きいため、電子部品がソルダーレジストに乗り上げることがなく、もって本発明の電子ユニットによれば、配線基板と電子部品との接合性の低下を未然に防止できる。

【００７０】請求項６に関わる電子部品実装方法では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンの表面を覆うソルダーレジストに、表層の配線パターンに実装される電子部品の外形よりも大きい開口を形成して成る配線基板に、異方性導電接合材料を介して電子部品を実装する電子部品実装方法において、配線基板の実装面にフィルム状の異方性導電接合材料を載置する工程と、フィルム状の異方性導電接合材料をヒートツールの柔軟性および耐熱性を備えたパッドにより加圧および加熱して配線基板の実装面に仮付けする工程とを含んでいる。上記構成によれば、表層の配線パターンの直下における絶縁層の剛性が向上するため、配線基板への加熱および加圧に対する前記絶縁層の変形、延いては前記配線パターンの変形が可及的に抑えられ、もって本発明の電子部品実装方法によれば、配線基板と電子部品との接合性の低下を未然に防止できる。さらに上記構成では、ヒートツールにおけるパッドの柔軟性により、フィルム状の異方性導電接合材料を、配線基板の実装面に追従させて確実に仮接着でき、もって本発明の電子部品実装方法によれば、配線基板と電子部品との接合性の低下を未然に防止できる。

【００７１】請求項７に関わる配線基板では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンにおける電極を、先端部のコーナーを切欠いた形状としている。上記構成によれば、表層の配線パターンの直下における絶縁層の剛性が向上するため、配線基板への加熱および加圧に対する前記絶縁層の変形、延いては前記配線パターンの変形が可及的に抑えられ、もって本発明の配線基板によれば、配線基板と電子部品との接合性の低下を未然に防止できる。さらに上記構成によれば、電

極を先端部のコーナーを切欠いた形状としたことで、コーナー部分において隣接する電極同士のショートを防止しつつ電極を大型化することができ、かつ溶融した異方性導電接合材料が配線パターン間に流入し易いものとなり、もって本発明の配線基板によれば、配線基板と電子部品との接合性の低下を未然に防止できる。

【００７２】請求項８に関わる電子ユニットでは、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンにおける電極を、先端部のコーナーを切欠いた形状として成る配線基板に、異方性導電接合材料を介して電子部品を実装している。上記構成によれば、表層の配線パターンの直下における絶縁層の剛性が向上するため、配線基板への加熱および加圧に対する前記絶縁層の変形、延いては前記配線パターンの変形が可及的に抑えられ、もって本発明の電子ユニットによれば配線基板と電子部品との接合性の低下を未然に防止できる。さらに上記構成によれば、電極を先端部のコーナーを切欠いた形状としたことで、コーナー部分において隣接する電極同士のショートを防止しつつ電極を大型化することができ、かつ溶融した異方性導電接合材料が配線パターン間に流入し易いものとなり、もって本発明の電子ユニットによれば、配線基板と電子部品との接合性の低下を未然に防止できる。

【００７３】請求項９に関わる電子部品実装方法では、絶縁層を挟んで積層された配線パターンを具備し、表層の配線パターンの直下における絶縁層を、ガラスクロスに樹脂を含浸させて形成するとともに、この表層の配線パターンにおける電極を、先端部のコーナーを切欠いた形状として成る配線基板に、異方性導電接合材料を介して電子部品を実装する電子部品実装方法であって、配線基板の実装面にフィルム状の異方性導電接合材料を載置する工程と、フィルム状の異方性導電接合材料をヒートツールの柔軟性および耐熱性を備えたパッドにより加圧および加熱して配線基板の実装面に仮付けする工程とを含んでいる。上記構成によれば、表層の配線パターンの直下における絶縁層の剛性が向上するため、配線基板への加熱および加圧に対する前記絶縁層の変形、延いては前記配線パターンの変形が可及的に抑えられ、もって本発明の電子部品実装方法によれば、配線基板と電子部品との接合性の低下を未然に防止できる。さらに上記構成によれば、電極を先端部のコーナーを切欠いた形状としたことで、コーナー部分において隣接する電極同士のショートを防止しつつ電極を大型化することができ、かつ溶融した異方性導電接合材料が配線パターン間に流入し易いものとなり、もって本発明の電子部品実装方法によれば、配線基板と電子部品との接合性の低下を未然に防止できる。さらに上記構成では、ヒートツールにおけるパッドの柔軟性により、フィルム状の異方性導電接合材料を、配線基板の実装面に追従させて確実に仮接着でき、もって本発明の電子部品実装方法によれば、配線基板と電子部品との接合性の低下を未然に防止できる。

【図面の簡単な説明】

【図１】（ａ）および（ｂ）は、本発明に関わる電子ユニットを示す要部平面図および要部断面側面図。

【図２】（ａ）および（ｂ）は、本発明に関わる配線基板を示す要部平面図および要部断面側面図。

【図３】本発明に関わる配線基板における電極の形状を示す要部平面図。

【図４】（ａ）および（ｂ）は、本発明に関わる配線基板における電極の形状の他の例を示す要部平面図。

【図５】本発明に関わる電子ユニットの製造工程を概念的に示す断面側面図。

【図６】本発明に関わる電子ユニットの製造工程を概念的に示す断面側面図。

【図７】本発明に関わる電子ユニットの製造工程を概念的に示す断面側面図。

【図８】本発明に関わる電子ユニットの製造工程を概念的に示す断面側面図。

【図９】従来の電子ユニットを示す要部断面側面図。

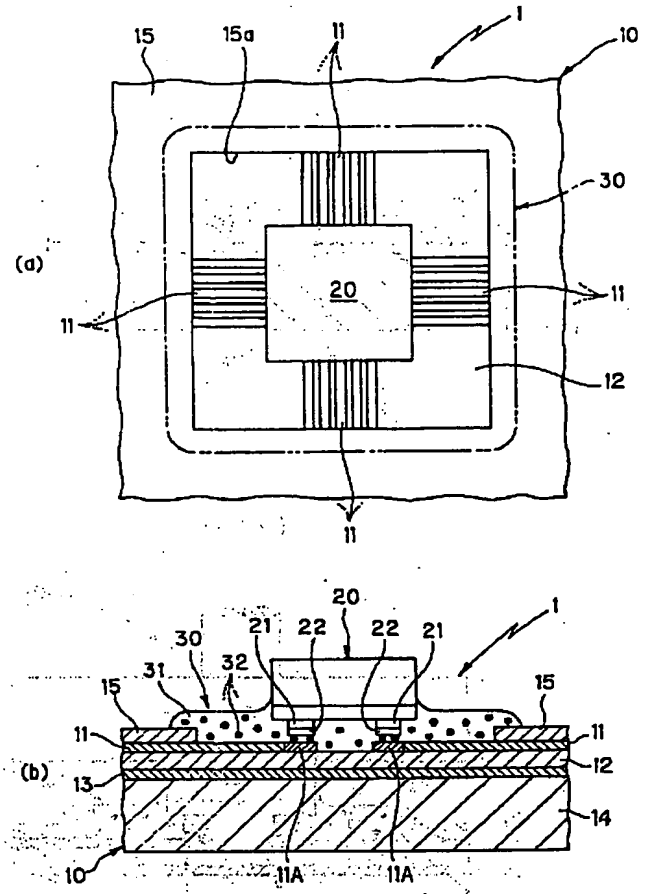
【図１０】従来の配線基板を示す要部平面図。

【図１１】（ａ）および（ｂ）は、従来の電子ユニットの製造工程を示す概念図。

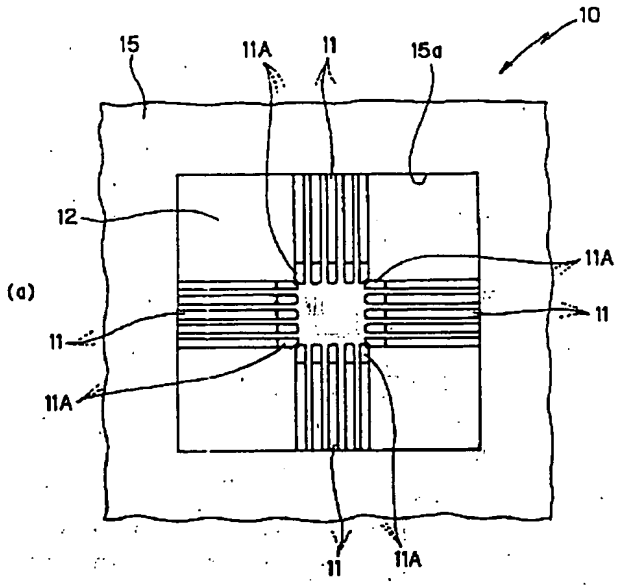
【符号の説明】

１…電子ユニット、
１０…配線基板、
１１…表層の配線パターン、
１１Ａ…電極、
１２…絶縁層、
１５…ソルダーレジスト、
１５ａ…開口、
２０…ベアＩＣチップ（電子部品）、
３０…異方性導電接合材料、
４０…ヒートツール、
４１…パッド。

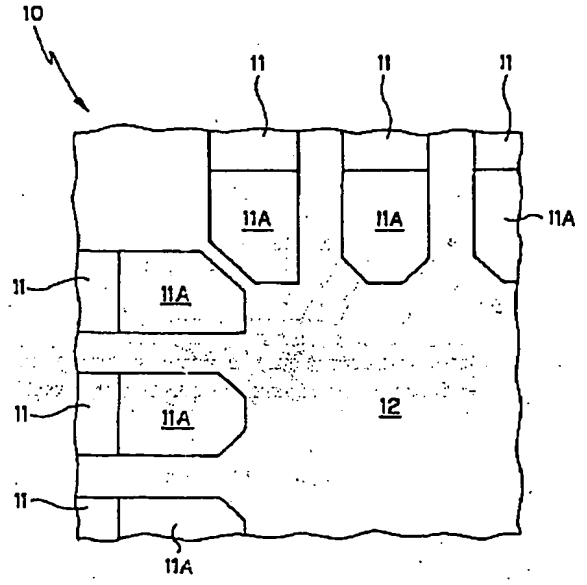
【図１】


15
15a
11
1
10
30
20
(a)
11
12
(b)
13
14
21
22
31
32
11A

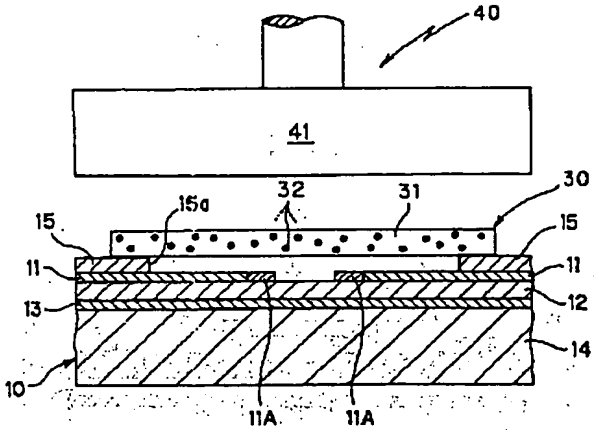
【図２】


10
15
11A
11
15a
12
(a)
11A
11
(b)
13
14
15
15a
11
11A
12

【図３】


10
11
11A
12

【図５】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15a
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11A
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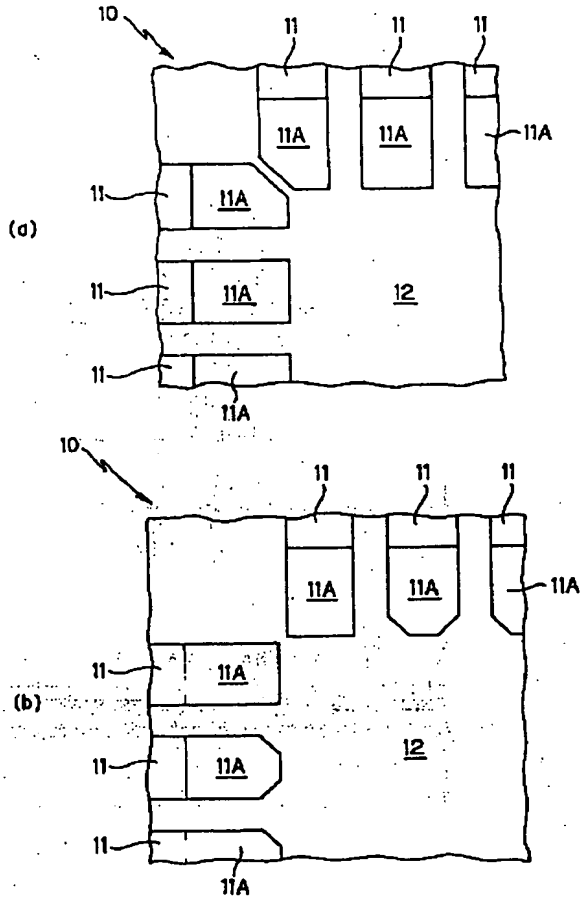
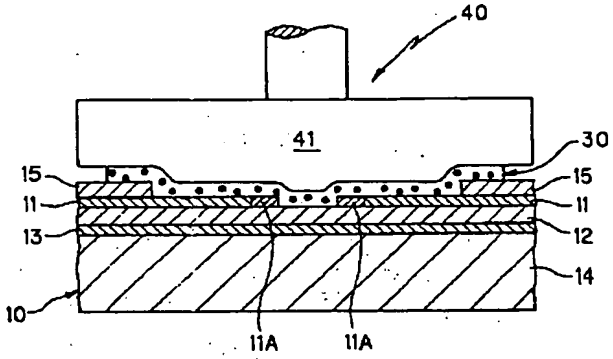
10

【図４】


(a)
(b)
10
11
11A
12

【図６】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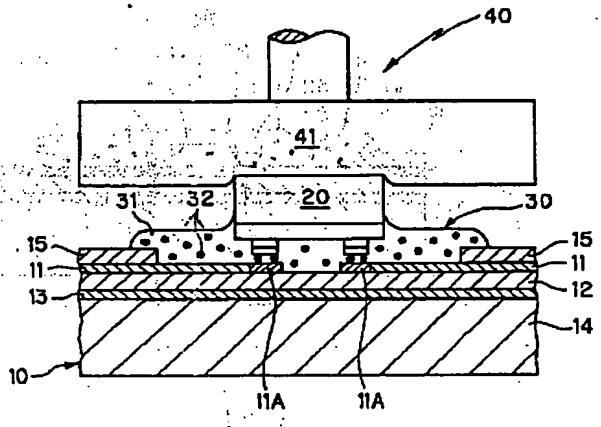
11A

【図８】


40
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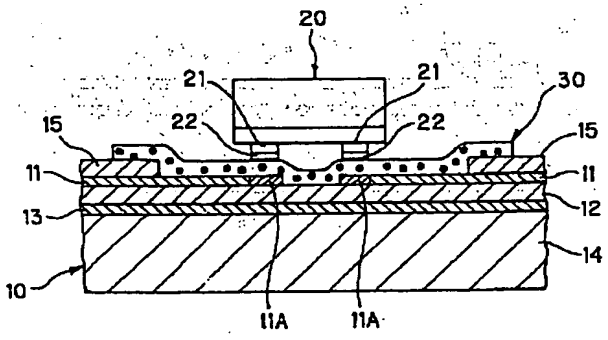
11A

【図７】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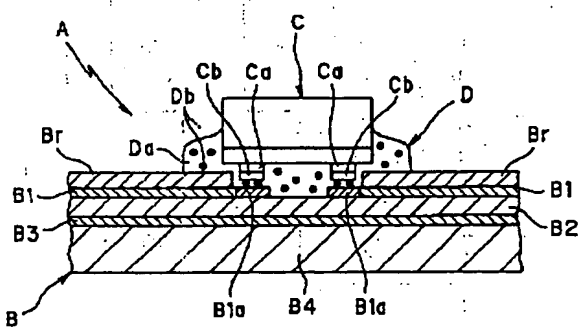
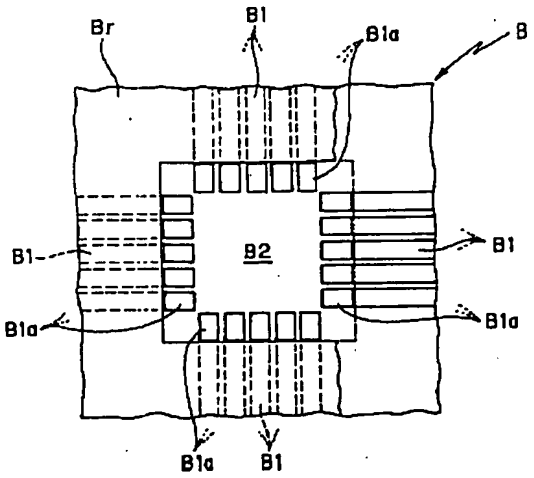
11A

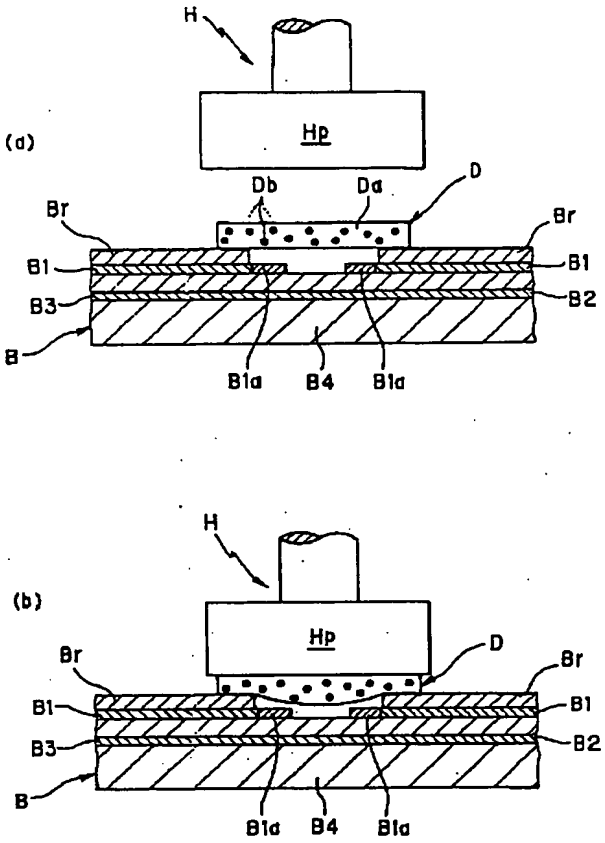
【図９】


A
C
Cb
Ca
Db
D
Da
Br
B1
B2
B3
B
B1a
B4

【図１０】



【図１１】



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(71)Applicant : TOSHIBA CORP

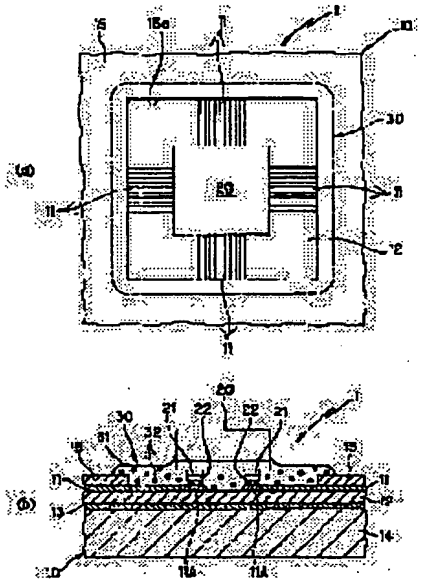
(72)Inventor : TAKIZAWA MINORU

(54) WIRING BOARD AND ELECTRONIC UNIT, AND METHOD OF MOUNTING ELECTRONIC PARTS

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a wiring board and an electronic unit which can prevent the drop of junction property between the wiring board and the electronic parts, and a method for mounting electronic parts.

SOLUTION: For a wiring board 10, an insulating layer 12 right under the wiring pattern at the surface is made, impregnating glass cloth with resin. Moreover, for an electronic unit 11, a bare IC chip 20 is mounted through anisotropic conductive junction material 30 on the wiring board 10 where the insulating layer 12 right under the wiring pattern 11 at the surface layer is made by impregnating glass cloth with resin. Moreover, an electronic parts mounting method includes a process of placing film-shaped anisotropic conductive junction material 3 on the mounting face of the wiring board 10, and a process of temporarily fixing the film-shaped anisotropic conductive junction material 30 on the mounting face of the wiring board 10 by pressurizing and heating it by means of the flexible and heat-resistant pad of a heat tool.



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CLAIMS

[Claim(s)]

[Claim 1] The wiring substrate which is a wiring substrate of the build up mold manufactured by providing the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and carrying out the laminating of said circuit pattern and said insulating layer one by one, and is characterized by having infiltrated the insulating layer in directly under [of a surface circuit pattern] into glass fabrics, and forming resin in them for it.

[Claim 2] The electronic unit characterized by mounting electronic parts in the wiring substrate of the build up mold manufactured by providing the circuit pattern by which the laminating was carried out on both sides of the insulating layer, infiltrating resin into glass fabrics, forming the insulating layer in directly under [of a surface circuit pattern], and carrying out the laminating of said circuit pattern and said insulating layer one by one, and growing into it through an anisotropy electric conduction cementing material.

[Claim 3] Provide the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and the insulating layer in directly under [of a surface circuit pattern] Infiltrate resin into glass fabrics, form and said circuit pattern and said insulating layer to the wiring substrate of the build up mold manufactured by carrying out a laminating one by one The process which is the electronic-parts mounting approach of mounting electronic parts through an anisotropy electric conduction cementing material, and lays a film-like anisotropy electric conduction cementing material in the component side of said wiring substrate, The electronic-parts mounting approach characterized by pressurizing and heating the anisotropy electric conduction cementing material of the shape of said film with the pad equipped with the flexibility of a heat tool, and thermal resistance, and growing into the component side of said wiring substrate including the process which carries out temporary attachment.

[Claim 4] The wiring substrate which possesses the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and is characterized by forming larger opening than the appearance of the electronic parts mounted in the circuit pattern of said surface by the wrap solder resist in the front face of the circuit pattern of said surface while infiltrating the insulating layer in directly under [of a surface circuit pattern] into glass fabrics and forming resin in them.

[Claim 5] The electronic unit characterized by providing the circuit pattern by which the laminating was carried out on both sides of the insulating layer, mounting electronic parts in the wiring substrate which forms large opening and changes, and changing from the appearance of the electronic parts mounted in the circuit pattern of said surface by the wrap solder resist in the front face of the circuit pattern of said surface to it through an anisotropy electric conduction cementing material while infiltrating the insulating layer in directly under [of a surface circuit pattern] into glass fabrics and forming resin in them.

[Claim 6] While providing the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and the insulating layer in directly under [of a surface circuit pattern] infiltrating resin into glass fabrics and forming Larger opening than the appearance of the electronic parts mounted in the circuit pattern of said surface by the wrap solder resist in the front face of the circuit pattern of said surface to the wiring substrate which forms and changes The process which is the electronic-parts

mounting approach of mounting electronic parts through an anisotropy electric conduction cementing material, and lays a film-like anisotropy electric conduction cementing material in the component side of said wiring substrate, The electronic-parts mounting approach characterized by pressurizing and heating the anisotropy electric conduction cementing material of the shape of said film with the pad equipped with the flexibility of a heat tool, and thermal resistance, and growing into the component side of said wiring substrate including the process which carries out temporary attachment.

[Claim 7] The wiring substrate which possesses the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and is characterized by making the corner of a point into a notching **** configuration for the electrode in the circuit pattern of said surface while infiltrating the insulating layer in directly under [of a surface circuit pattern] into glass fabrics and forming resin in them.

[Claim 8] The electronic unit which possesses the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and is characterized by mounting electronic parts in the wiring substrate which changes the electrode in the circuit pattern of said surface considering the corner of a point as a notching **** configuration, and growing into it through an anisotropy electric conduction cementing material while infiltrating the insulating layer in directly under [of a surface circuit pattern] into glass fabrics and forming resin in them.

[Claim 9] While providing the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and the insulating layer in directly under [of a surface circuit pattern] infiltrating resin into glass fabrics and forming The electrode in the circuit pattern of said surface to the wiring substrate which changes considering the corner of a point as a notching **** configuration The process which is the electronic-parts mounting approach of mounting electronic parts through an anisotropy electric conduction cementing material, and lays a film-like anisotropy electric conduction cementing material in the component side of said wiring substrate, The electronic-parts mounting approach characterized by pressurizing and heating the anisotropy electric conduction cementing material of the shape of said film with the pad equipped with the flexibility of a heat tool, and thermal resistance, and growing into the component side of said wiring substrate including the process which carries out temporary attachment.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the electronic-parts mounting approach at the time of manufacturing the wiring substrate possessing the circuit pattern by which the laminating was carried out on both sides of the insulating layer, the electronic unit which mounts electronic parts in this wiring substrate, and grows into it, and this electronic unit.

[0002]

[Description of the Prior Art] There is the flip chip mounting approach (the flip-chip-bonding method) using the anisotropy electric conduction cementing material as one of the approaches which mounts the semiconductor device which is electronic parts in a wiring substrate (printed wired board).

[0003] Drawing 9 is electronic unit A manufactured using the flip chip mounting approach, and the raise in basic wages IC chip C which is electronic parts is mounted in the wiring substrate B through the anisotropy electric conduction cementing material D.

[0004] As shown in drawing 10 , the circuit pattern B1 with which the laminating of a circuit pattern and the insulating layer is carried out by turns, and the wiring substrate B changes from an electrical conducting material to a component side (drawing Nakagami side), and B1 — are formed, and electrode B1a is respectively formed at the tip of each circuit pattern B1 of gold plate.

[0005] Insulating-layer B-2 formed from insulating resin is formed directly under the surface circuit pattern B1, a circuit pattern B3 is formed directly under this insulating-layer B-2, and insulating-layer B4 is further formed directly under the circuit pattern B3.

[0006] Moreover, as shown in drawing 10 , the surface circuit pattern B1 and B1 — are covered with the solder resist Br in the front face except for the part of each electrode B1a.

[0007] On the other hand, the electrode calcium corresponding to the component side (drawing insole side) and calcium— are prepared with electrode B1a of the wiring substrate B, and B1a—, and the raise in basic wages IC chips C which are electronic parts as shown in drawing 9 are each electrodes calcium and calcium. — Bump Cb is respectively formed in the front face.

[0008] In order to manufacture electronic unit A mentioned above, as shown in drawing 11 (a), the film-like anisotropy electric conduction cementing material (anisotropy electric conduction film) D is first laid in the component side of the wiring substrate B. In addition, the anisotropy electric conduction cementing material D is formed like common knowledge by making the electric conduction particle Db and Db— intermingled to insulating resin Da.

[0009] Subsequently, as shown in drawing 11 (b), the anisotropy electric conduction cementing material D is pressurized from heating and the upper part with the heat tool H, and temporary adhesion of the anisotropy electric conduction cementing material D is carried out at the wiring substrate B. In addition, the pad Hp of the heat tool H is formed from metallic materials, such as stainless steel, and the heater for heating which is not illustrated is formed in the interior.

[0010] Subsequently, after laying the raise in basic wages IC chip C which is not illustrated to the anisotropy electric conduction cementing material D by which temporary adhesion was carried out in the wiring substrate B, actual adhesion of the raise in basic wages IC chip C is carried out at the wiring substrate B by pressurizing the raise in basic wages IC chip C with the heat tool H, and heating the anisotropy electric conduction cementing material D.

[0011] According to the thing which write and to do, the raise in basic wages IC chip C is joined to the wiring substrate B with the insulating resin Da of the anisotropy electric conduction cementing material D, and it connects electrically because the electric conduction particle Db of the anisotropy electric conduction cementing material D and Db— intervene between each electrode calcium of each electrode B1a of the wiring substrate B, and the raise in basic wages IC chip C (bump Cb).

[0012]

[Problem(s) to be Solved by the Invention] By the way, the wiring substrate B which constitutes the conventional electronic unit A Since the surface circuit pattern B1 and insulating-layer B-2 of B1 — located in directly under are formed from insulating resin, Further, when above-mentioned insulating-layer B-2 deforms under the pressurization at the pressurization at the time of carrying out temporary adhesion of the anisotropy electric conduction cementing material D and heating, and the time of carrying out actual adhesion of the raise in basic wages IC chip C at the wiring substrate B, and the effect of heating, the surface circuit pattern B1 and electrode B1a will deform into the wiring substrate B.

[0013] Thereby, there was un-arranging [to which the junction nature of the raise in basic wages IC

chip C to the wiring substrate B, i.e., the mechanical junction nature by the insulating resin Da of the anisotropy electric conduction cementing material D, and the electric junction nature by the electric conduction particle Db of the anisotropy electric conduction cementing material D fall].

[0014] This invention aims at offer of the possible wiring substrate and possible electronic unit of preventing beforehand the fall of the junction nature of the wiring substrate and electronic parts resulting from deformation of a surface of the insulating layer directly under a circuit pattern in view of the above-mentioned actual condition, and the electronic-parts mounting approach.

[0015] On the other hand, since the solder resist Br has covered the surface circuit pattern B1 and B1 — in the mode which makes only electrode B1a and B1a— expose as shown in drawing 9 and drawing 10 , when the wiring substrate B which constitutes the conventional electronic unit A mounts the raise in basic wages IC chip C in the wiring substrate B, it has a possibility that the edge base of the raise in basic wages IC chip C may run aground to a solder resist Br.

[0016] The connection through the electric conduction particle Db of the anisotropy electric conduction cementing material D of each electrode B1a in the wiring substrate B and each electrode calcium in the raise in basic wages IC chip C (bump Cb) became imperfect by this, and there was un-arranging [to which the junction nature of the raise in basic wages IC chip C to the wiring substrate B falls].

[0017] This invention aims at offer of the possible wiring substrate and possible electronic unit of preventing beforehand the fall of the junction nature of the wiring substrate and electronic parts resulting from the configuration of a solder resist in view of the above-mentioned actual condition, and the electronic-parts mounting approach.

[0018] It is desirable to, make the tip of electrode B1a extend on the other hand, in order for the flat-surface configuration of electrode B1a in each circuit pattern B1 to present the shape of a rectangle, to raise the electric connection effectiveness of the wiring substrate B and the raise in basic wages IC chip C and to increase a touch area, as the wiring substrate B which constitutes the conventional electronic unit A shows to drawing 10 .

[0019] However, since there was a possibility that the electrodes which adjoin in a corner part may interfere and short-circuit, difficultly, enlarging electrode B1a of a circuit pattern B1 had, and it was obliged to the fall of electric connectability.

[0020] moreover, be hard flow among the circuit patterns B1 and B1 with which the insulating resin Da of the fused anisotropy electric conduction cementing material D adjoin the wiring substrate B at the process which carry out actual adhesion of the raise in basic wages IC chip C since the point of electrode B1a in each circuit pattern B1 be square from a tip side, and there be un-arrange [which there be a possibility may produce a void, have in insulating resin Da, and cause the fall of mechanical connectability].

[0021] This invention aims at offer of the possible wiring substrate and possible electronic unit of preventing beforehand the fall of the junction nature of the wiring substrate and electronic parts resulting from the configuration of the electrode in a circuit pattern in view of the above-mentioned actual condition, and the electronic-parts mounting approach.

[0022] On the other hand, in case the conventional electronic unit A is manufactured, since Pad Hp is formed from hard metallic materials, such as stainless steel, as mentioned above, as the heat tool H used for the wiring substrate B at the process which carries out temporary adhesion of the anisotropy electric conduction cementing material D is shown in drawing 11 (b), the anisotropy electric conduction cementing material D is not followed at the component side of the wiring substrate B with which the laminating of each circuit pattern B1 (electrode B1a) or the solder resist Br was carried out.

[0023] For this reason, positive temporary adhesion of the anisotropy electric conduction cementing material D to the wiring substrate B was not performed, but this adhesion with the wiring substrate B in a next process and the raise in basic wages IC chip C became imperfect, and there was un-arranging [to which the junction nature of the raise in basic wages IC chip C to the wiring substrate B falls].

[0024] This invention aims at offer of the electronic-parts mounting approach which can prevent

beforehand the fall of the junction nature of the wiring substrate and electronic parts resulting from the quality of the material of a heat tool in view of the above-mentioned actual condition.
[0025]
[Means for Solving the Problem] In the wiring substrate in connection with claim 1, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, in the wiring substrate of the build up mold manufactured by carrying out the laminating of this circuit pattern and insulating layer one by one, resin is infiltrated into glass fabrics and the insulating layer in directly under [of a surface circuit pattern] is formed in them in order to attain the above-mentioned purpose.
[0026] Moreover, in the electronic unit in connection with claim 2, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, resin is infiltrated into glass fabrics, the insulating layer in directly under [of a surface circuit pattern] is formed, and electronic parts are mounted in the wiring substrate of the build up mold manufactured by carrying out the laminating of this circuit pattern and insulating layer one by one through an anisotropy electric conduction cementing material.
[0027] moreover, by the electronic-parts mounting approach in connection with claim 3 Provide the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and the insulating layer in directly under [of a surface circuit pattern] In the electronic-parts mounting approach of mounting electronic parts in the wiring substrate of the build up mold manufactured by infiltrating resin into glass fabrics, forming and carrying out the laminating of this circuit pattern and insulating layer one by one through an anisotropy electric conduction cementing material The process which pressurizes and heats the process which lays a film-like anisotropy electric conduction cementing material in the component side of a wiring substrate, and a film-like anisotropy electric conduction cementing material with the pad equipped with the flexibility of a heat tool and thermal resistance, and carries out temporary attachment at the component side of a wiring substrate is included.
[0028] Moreover, in the wiring substrate in connection with claim 4, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, and while infiltrating resin into glass fabrics and forming the insulating layer in directly under [of a surface circuit pattern] in them, larger opening than the appearance of the electronic parts mounted in a surface circuit pattern by the wrap solder resist in the front face of the circuit pattern of this surface is formed.
[0029] Moreover, in the electronic unit in connection with claim 5, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, and while infiltrating resin into glass fabrics and forming the insulating layer in directly under [of a surface circuit pattern] in them, electronic parts are mounted in the wiring substrate which forms large opening and consists of the appearance of the electronic parts mounted in a surface circuit pattern by the wrap solder resist in the front face of the circuit pattern of this surface through an anisotropy electric conduction cementing material.
[0030] moreover, by the electronic-parts mounting approach in connection with claim 6 While providing the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and the insulating layer in directly under [of a surface circuit pattern] infiltrating resin into glass fabrics and forming Larger opening than the appearance of the electronic parts mounted in a surface circuit pattern by the wrap solder resist in the front face of the circuit pattern of this surface to the wiring substrate which forms and changes In the electronic-parts mounting approach of mounting electronic parts through an anisotropy electric conduction cementing material The process which pressurizes and heats the process which lays a film-like anisotropy electric conduction cementing material in the component side of a wiring substrate, and a film-like anisotropy electric conduction cementing material with the pad equipped with the flexibility of a heat tool and thermal resistance, and carries out temporary attachment at the component side of a wiring substrate is included.
[0031] Moreover, in the wiring substrate in connection with claim 7, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, and while infiltrating resin

into glass fabrics and forming the insulating layer in directly under [of a surface circuit pattern] in them, the corner of a point is made into the notching **** configuration for the electrode in the circuit pattern of this surface.

[0032] Moreover, in the electronic unit in connection with claim 8, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, and while infiltrating resin into glass fabrics and forming the insulating layer in directly under [of a surface circuit pattern] in them, electronic parts are mounted in the wiring substrate which changes the electrode in the circuit pattern of this surface considering the corner of a point as a notching **** configuration through an anisotropy electric conduction cementing material.

[0033] moreover, by the electronic-parts mounting approach in connection with claim 9 While providing the circuit pattern by which the laminating was carried out on both sides of the insulating layer, and the insulating layer in directly under [of a surface circuit pattern] infiltrating resin into glass fabrics and forming The electrode in the circuit pattern of this surface to the wiring substrate which changes considering the corner of a point as a notching **** configuration The process which is the electronic-parts mounting approach of mounting electronic parts through an anisotropy electric conduction cementing material, and lays a film-like anisotropy electric conduction cementing material in the component side of a wiring substrate, A film-like anisotropy electric conduction cementing material is pressurized and heated with the pad equipped with the flexibility of a heat tool, and thermal resistance, and the process which carries out temporary attachment is included in the component side of a wiring substrate.

[0034]

[Embodiment of the Invention] Hereafter, this invention is explained to a detail based on the drawing in which one example is shown. Drawing 1 (a) and (b) show the electronic unit 1 in connection with this invention manufactured using the flip chip mounting approach, and it has the wiring substrate 10 and the raise in basic wages IC chip 20 as electronic parts, and using the anisotropy electric conduction cementing material 30, this electronic unit 1 mounts the raise in basic wages IC chip 20 in the wiring substrate 10, and is constituted.

[0035] Moreover, said electronic unit 1 is manufactured through the process which lays the anisotropy electric conduction cementing material 30 in the wiring substrate 10, the process which similarly carries out temporary adhesion of the anisotropy electric conduction cementing material 30, the process which lays the raise in basic wages IC chip 20 in the anisotropy electric conduction cementing material 30, and the process which carries out actual adhesion of the raise in basic wages IC chip 20 at the wiring substrate 10 so that it may explain in full detail behind.

[0036] The wiring substrate 10 which constitutes an electronic unit 1 is the so-called build up type manufactured by carrying out the laminating of two or more circuit patterns and insulating layers which are mentioned later one by one of wiring substrate (build up substrate), and as shown in drawing 1 and drawing 2 , the surface circuit pattern 11 and 11 — are formed in the component side (drawing Nakagami side) of the wiring substrate 10.

[0037] The insulating layer 12 is formed in directly under, and this insulating layer 12 is formed in it by [of the circuit pattern 11 of said surface, and 11 —] infiltrating resin into glass fabrics. Moreover, a circuit pattern 13 is formed directly under an insulating layer 12, and the insulating layer 14 is further formed directly under the circuit pattern 13.

[0038] The circuit pattern 11 of the surface in the wiring substrate 10 and 11 — are formed from the electrical conducting material, and electrode 11A and 11A— is formed at the tip by [of each circuit pattern 11 and 11 —] performing gold plate. Moreover, electrode 11A in each circuit pattern 11 is presenting the notching **** configuration for the corner of a point, as shown in drawing 3 .

[0039] As shown in drawing 1 and drawing 2 , it is greatly formed by covering the front face with the solder resist 15 at this solder resist 15 for [appearance / of the circuit pattern 11 of the surface in the wiring substrate 10, and 11 — / of the raise in basic wages IC chip 20 with which opening 15a of said

circuit pattern 11 and 11 — which makes electrode 11A and 11A— expose is mounted in the wiring substrate 10] whether being Haruka.
[0040] In addition, the wiring substrate 10 of a configuration of having mentioned above may not be limited to the wiring substrate of a build up mold, and may be a **** usual wiring substrate manufactured by carrying out thermocompression bonding of the formed substrate unit and the substrate unit which formed the circuit pattern 11 in the insulating layer 12 in piles mutually circuit pattern 13 at an insulating layer 14.
[0041] On the other hand, as the raise in basic wages IC chip 20 as electronic parts is shown in drawing 1 (b), the wiring substrate 10, the electrode 21 which changes from electrical conducting materials, such as aluminum (aluminum), to the component side (drawing insole side) which counters, and 21 — are formed.
[0042] It is arranged corresponding to each electrode 11A in the wiring substrate 10, and 11A—, and these electrodes 21 and 21 — are the electrodes 21 and 21 of the raise in basic wages IC chip 20. — A bump 22 and 22 — are formed in the front face with Au(gold) or a Sn-Pb (tin-lead) alloy.
[0043] Below, the mounting approach of the approach of manufacturing the electronic unit 1 of a configuration of having mentioned above, and the raise in basic wages IC chip 20 to as opposed to [in other words] the wiring substrate 10 is explained.
[0044] First, as shown in drawing 5 , the film-like anisotropy electric conduction cementing material (anisotropy electric conduction film) 30 is laid in the component side of the wiring substrate 10. Here, the anisotropy electric conduction cementing material 30 makes the electric conduction particle 32 and 32 — intermingled to insulating resin 31, and is formed in the shape of a film, and as shown in drawing 5 , it fully has wrap magnitude for opening 15a of a solder resist 15.
[0045] Subsequently, as shown in drawing 6 , the film-like anisotropy electric conduction cementing material 30 is pressurized from heating and the upper part with the heat tool 40, and temporary adhesion of the anisotropy electric conduction cementing material 30 is carried out at the wiring substrate 10.
[0046] Here, the heat tool 40 is equipped with the pad 41 having the heater for heating which is not illustrated, and this pad 41 is constituted by ingredients possessing flexibility and thermal resistance, such as for example, silicon system heatproof resin and Teflon system heatproof resin.
[0047] For this reason, when the anisotropy electric conduction cementing material 30 is pressurized with a pad 41, and a pad 41 deforms, the whole anisotropy electric conduction cementing material 30 will stick to the component side of the wiring substrate 10, and temporary adhesion of the anisotropy electric conduction cementing material 30 will be certainly carried out to the wiring substrate 10.
[0048] Subsequently, as shown in drawing 7 , the raise in basic wages IC chip 20 is laid in the anisotropy electric conduction cementing material 30 by which temporary adhesion was carried out. At this time, the raise in basic wages IC chip 20 is laid in the anisotropy electric conduction cementing material 30 in the location mode which makes each electrode 21 (bump 22) of the raise in basic wages IC chip 20 correspond to each electrode 11A of the wiring substrate 10.
[0049] Then, as shown in drawing 8 , while pressurizing the raise in basic wages IC chip 20 using the same heat tool 40 with having carried out temporary adhesion of the anisotropy electric conduction cementing material 30 previously, actual adhesion of the raise in basic wages IC chip 20 is carried out by heating the anisotropy electric conduction cementing material 30 at the wiring substrate 10.
[0050] The wiring substrate 10 and the raise in basic wages IC chip 20 are joined in this way with the insulating resin 31 of the anisotropy electric conduction cementing material 30 hardened after fusing, and it connects electrically because the electric conduction particle 32 of the anisotropy electric conduction cementing material 30 and 32 — intervene between each electrode 11A of the wiring substrate 10, and each electrode 21 (bump 22) of the raise in basic wages IC chip 20.
[0051] As mentioned above, when it mounts the raise in basic wages IC chip 20 in the wiring substrate 10, in case actual adhesion of the raise in basic wages IC chip 20 is carried out, pressurization and

heating will act on the wiring substrate 10 in case temporary adhesion of the anisotropy electric conduction cementing material 30 is carried out at the wiring substrate 10 to the wiring substrate 10.
[0052] On the other hand, since the insulating layer 12 located directly under the circuit pattern 11 of the surface in the wiring substrate 10 infiltrates resin into glass fabrics and is formed in them, rigidity is improving compared with the insulating layer formed from conventional insulating resin, and deformation of the insulating layer 12 to heating and pressurization to the wiring substrate 10, as a result deformation of a circuit pattern 11 (electrode 11A) are suppressed as much as possible.
[0053] Thereby, the fall of the junction nature of the raise in basic wages IC chip 20 to the wiring substrate 10, i.e., the mechanical junction nature by the insulating resin 31 of the anisotropy electric conduction cementing material 30, and the electric junction nature by the electric conduction particle 32 of the anisotropy electric conduction cementing material 30 can be prevented beforehand.
[0054] Moreover, by the former, as mentioned above, when it mounts the raise in basic wages IC chip 20 in the wiring substrate 10, since larger opening 15a than the appearance of the raise in basic wages IC chip 20 is formed in the solder resist 15 in the wiring substrate 10 to there having been a possibility that the edge base of a raise in basic wages IC chip might run aground to a solder resist, the raise in basic wages IC chip 20 does not run aground to a solder resist 15.
[0055] For this reason, it becomes possible to connect certainly through the electric conduction particle 32 of the anisotropy electric conduction cementing material 30, and for each electrode 11A of the wiring substrate 10 and each electrode 21 (bump 22) of the raise in basic wages IC chip 20 to have, and to prevent beforehand the fall of the junction nature of the raise in basic wages IC chip 20 to the wiring substrate 10.
[0056] Furthermore, in the condition that the electronic unit 1 was completed, since opening 15a of a solder resist 15 is not what is closed using special insulating resin while the closure of the surface circuit pattern 11 is carried out and it is protected from oxidation or external force, without exposing into atmospheric air, since it is covered with the anisotropy electric conduction cementing material 30 as shown in drawing 1 , it does not make the production process of an electronic unit 1 complicated to ** and others.
[0057] Moreover, as mentioned above, since the circuit pattern 11 of the surface in the wiring substrate 10 and the electrodes 11A and 11A of 11 — which are presenting the notching **** configuration and adjoin the corner of a point especially in a corner part as electrode 11A and 11A— is shown in drawing 3 are presenting the notching **** configuration for the corner which counters, they have attained enlargement of each electrode 11A, preventing mutual short-circuit.
[0058] Furthermore, since electrode 11A other than the corner part mentioned above and 11A— are presenting the notching **** configuration for both the corners of the right and left in a point, the insulating resin 31 of the anisotropy electric conduction cementing material 30 fused when carrying out actual adhesion of the raise in basic wages IC chip 20 will flow easily from a tip side among the adjoining circuit patterns 11 and 11.
[0059] Thereby, the electric connection effectiveness of the wiring substrate 10 and the raise in basic wages IC chip 20 and mechanical connectability improve, and become possible [having and preventing beforehand the fall of the junction nature of the raise in basic wages IC chip 20 to the wiring substrate 10].
[0060] In addition, if it aims only at enlargement of an electrode, as shown in drawing 4 (a), it will set to electrode 11A of each circuit pattern 11. Possible that only the electrodes 11A and 11A which adjoin especially in a corner part make a corner a notching **** configuration, and make other electrode 11A and 11A— the shape of a rectangle as another mode the electrodes 11A and 11A which adjoin in a corner part in electrode 11A of each circuit pattern 11 as shown in drawing 4 (b) — the shape of a rectangle — carrying out — other electrode 11A and 11A— notching of a corner — him — it is good also as a **** configuration.
[0061] Moreover, since the pad of a heat tool was metal in the former when it mounted the raise in

basic wages IC chip 20 in the wiring substrate 10 as mentioned above With having constituted the pad 41 of the heat tool 40 from an ingredient equipped with flexibility and thermal resistance to an anisotropy electric conduction cementing material having not followed the component side of a wiring substrate, and were not able to carry out temporary adhesion of the anisotropy electric conduction cementing material certainly to the wiring substrate It enabled it to stick the whole anisotropy electric conduction cementing material 30 to the wiring substrate 10, and to carry out temporary adhesion certainly.

[0062] For this reason, it becomes possible to be also able to carry out certainly this adhesion with the wiring substrate 10 and the raise in basic wages IC chip 20 in a next process, to have it, and to prevent beforehand the fall of the junction nature of the raise in basic wages IC chip 20 to the wiring substrate 10.

[0063] Moreover, by having used the heat tool 40 mentioned above, also when making the wiring substrate 10 carry out actual adhesion of the raise in basic wages IC chip 20 Even when the raise in basic wages IC chip 20 is inclined and laid in the wiring substrate 10 to the anisotropy electric conduction cementing material 30 by which temporary adhesion was carried out It becomes possible to press the raise in basic wages IC chip 20 to homogeneity, to have it, and to connect certainly the raise in basic wages IC chip 20 of it to the wiring substrate 10, the flexibility of the pad 41 in the heat tool 40 absorbing the above-mentioned inclination.

[0064] In addition, in the example mentioned above, although the raise in basic wages IC chip is illustrated as electronic parts mounted in a wiring substrate, if it is the electronic parts by which flip chip mounting is carried out to a wiring substrate, it cannot be overemphasized in the wiring substrate or electronic unit carrying various electronic parts other than a raise in basic wages IC chip that this invention can be applied effectively.

[0065]

[Effect of the Invention] As mentioned above, as explained in full detail, in the wiring substrate in connection with claim 1, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, in the wiring substrate of the build up mold manufactured by carrying out the laminating of this circuit pattern and insulating layer one by one, resin is infiltrated into glass fabrics and the insulating layer in directly under [of a surface circuit pattern] is formed in them. Since the rigidity of the insulating layer in directly under [of a surface circuit pattern] improves according to the above-mentioned configuration, deformation of said insulating layer to heating and pressurization to a wiring substrate, as a result deformation of said circuit pattern are suppressed as much as possible, and according to the wiring substrate of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by having.

[0066] In the electronic unit in connection with claim 2, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, resin is infiltrated into glass fabrics, the insulating layer in directly under [of a surface circuit pattern] is formed, and electronic parts are mounted in the wiring substrate of the build up mold manufactured by carrying out the laminating of this circuit pattern and insulating layer one by one through an anisotropy electric conduction cementing material. Since the rigidity of the insulating layer in directly under [of a surface circuit pattern] improves according to the above-mentioned configuration, deformation of said insulating layer to heating and pressurization to a wiring substrate, as a result deformation of said circuit pattern are suppressed as much as possible, it has, and according to the electronic unit of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be prevented beforehand.

[0067] By the electronic-parts mounting approach in connection with claim 3, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided. Infiltrate resin into glass fabrics and the insulating layer in directly under [of a surface circuit pattern] is formed in them. In the electronic-parts mounting approach of mounting electronic parts in the wiring substrate of the build up mold manufactured by carrying out the laminating of this circuit pattern and insulating layer one

by one through an anisotropy electric conduction cementing material The process which pressurizes and heats the process which lays a film-like anisotropy electric conduction cementing material in the component side of a wiring substrate, and a film-like anisotropy electric conduction cementing material with the pad equipped with the flexibility of a heat tool and thermal resistance, and carries out temporary attachment at the component side of a wiring substrate is included. Since the rigidity of the insulating layer in directly under [of a surface circuit pattern] improves according to the above-mentioned configuration, deformation of said insulating layer to heating and pressurization to a wiring substrate, as a result deformation of said circuit pattern are suppressed as much as possible, and according to the electronic-parts mounting approach of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by having. Furthermore, according to the electronic-parts mounting approach of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented with the above-mentioned configuration by making a film-like anisotropy electric conduction cementing material follow the component side of a wiring substrate, being able to carry out the temporary adhesion of it certainly, and having it according to the flexibility of the pad in a heat tool.

[0068] In the wiring substrate in connection with claim 4, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, and while infiltrating resin into glass fabrics and forming the insulating layer in directly under [of a surface circuit pattern] in them, larger opening than the appearance of the electronic parts mounted in a surface circuit pattern by the wrap solder resist in the front face of the circuit pattern of this surface is formed. Since the rigidity of the insulating layer in directly under [of a surface circuit pattern] improves according to the above-mentioned configuration, deformation of said insulating layer to heating and pressurization to a wiring substrate, as a result deformation of said circuit pattern are suppressed as much as possible, and according to the wiring substrate of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by having. Furthermore, according to the above-mentioned configuration, since opening of a solder resist is larger than the appearance of electronic parts, according to the wiring substrate of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by electronic parts' not running aground to a solder resist, and having.

[0069] In the electronic unit in connection with claim 5, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, and while infiltrating resin into glass fabrics and forming the insulating layer in directly under [of a surface circuit pattern] in them, electronic parts are mounted in the wiring substrate which forms large opening and consists of the appearance of the electronic parts mounted in a surface circuit pattern by the wrap solder resist in the front face of the circuit pattern of this surface through an anisotropy electric conduction cementing material. Since the rigidity of the insulating layer in directly under [of a surface circuit pattern] improves according to the above-mentioned configuration, deformation of said insulating layer to heating and pressurization to a wiring substrate, as a result deformation of said circuit pattern are suppressed as much as possible, it has, and according to the electronic unit of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be prevented beforehand. Furthermore, according to the above-mentioned configuration, since opening of a solder resist is larger than the appearance of electronic parts, according to the electronic unit of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by electronic parts' not running aground to a solder resist, and having.

[0070] While providing the circuit pattern by which the laminating was carried out on both sides of the insulating layer by the electronic-parts mounting approach in connection with claim 6, and the insulating layer in directly under [of a surface circuit pattern] infiltrating resin into glass fabrics and forming Larger opening than the appearance of the electronic parts mounted in a surface circuit pattern by the wrap solder resist in the front face of the circuit pattern of this surface to the wiring substrate which

forms and changes In the electronic-parts mounting approach of mounting electronic parts through an anisotropy electric conduction cementing material The process which pressurizes and heats the process which lays a film-like anisotropy electric conduction cementing material in the component side of a wiring substrate, and a film-like anisotropy electric conduction cementing material with the pad equipped with the flexibility of a heat tool and thermal resistance, and carries out temporary attachment at the component side of a wiring substrate is included. Since the rigidity of the insulating layer in directly under [of a surface circuit pattern] improves according to the above-mentioned configuration, deformation of said insulating layer to heating and pressurization to a wiring substrate, as a result deformation of said circuit pattern are suppressed as much as possible, and according to the electronic-parts mounting approach of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by having. Furthermore, according to the above-mentioned configuration, since opening of a solder resist is larger than the appearance of electronic parts, according to the electronic-parts mounting approach of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by electronic parts' not running aground to a solder resist, and having. Furthermore, according to the electronic-parts mounting approach of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented with the above-mentioned configuration by making a film-like anisotropy electric conduction cementing material follow the component side of a wiring substrate, being able to carry out the temporary adhesion of it certainly, and having it according to the flexibility of the pad in a heat tool.

[0071] In the wiring substrate in connection with claim 7, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, and while infiltrating resin into glass fabrics and forming the insulating layer in directly under [of a surface circuit pattern] in them, the corner of a point is made into the notching **** configuration for the electrode in the circuit pattern of this surface. Since the rigidity of the insulating layer in directly under [of a surface circuit pattern] improves according to the above-mentioned configuration, deformation of said insulating layer to heating and pressurization to a wiring substrate, as a result deformation of said circuit pattern are suppressed as much as possible, and according to the wiring substrate of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by having. According to the wiring substrate of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by the anisotropy electric conduction cementing material which could enlarge the electrode according to the above-mentioned configuration, preventing short-circuit of the electrodes which adjoin an electrode in a corner part by having considered as the notching **** configuration in the corner of a point, and was fused becoming what is easy to flow between circuit patterns, and furthermore, having.

[0072] In the electronic unit in connection with claim 8, the circuit pattern by which the laminating was carried out on both sides of the insulating layer is provided, and while infiltrating resin into glass fabrics and forming the insulating layer in directly under [of a surface circuit pattern] in them, electronic parts are mounted in the wiring substrate which changes the electrode in the circuit pattern of this surface considering the corner of a point as a notching **** configuration through an anisotropy electric conduction cementing material. Since the rigidity of the insulating layer in directly under [of a surface circuit pattern] improves according to the above-mentioned configuration, deformation of said insulating layer to heating and pressurization to a wiring substrate, as a result deformation of said circuit pattern are suppressed as much as possible, it has, and according to the electronic unit of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be prevented beforehand. According to the electronic unit of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by the anisotropy electric conduction cementing material which could enlarge the electrode according to the above-mentioned configuration, preventing short-circuit of the electrodes which adjoin an electrode in a corner part by having considered as the notching ****

configuration in the corner of a point, and was fused becoming what is easy to flow between circuit patterns, and furthermore, having.

[0073] While providing the circuit pattern by which the laminating was carried out on both sides of the insulating layer by the electronic-parts mounting approach in connection with claim 9, and the insulating layer in directly under [of a surface circuit pattern] infiltrating resin into glass fabrics and forming The electrode in the circuit pattern of this surface to the wiring substrate which changes considering the corner of a point as a notching **** configuration The process which is the electronic-parts mounting approach of mounting electronic parts through an anisotropy electric conduction cementing material, and lays a film-like anisotropy electric conduction cementing material in the component side of a wiring substrate, A film-like anisotropy electric conduction cementing material is pressurized and heated with the pad equipped with the flexibility of a heat tool, and thermal resistance, and the process which carries out temporary attachment is included in the component side of a wiring substrate. Since the rigidity of the insulating layer in directly under [of a surface circuit pattern] improves according to the above-mentioned configuration, deformation of said insulating layer to heating and pressurization to a wiring substrate, as a result deformation of said circuit pattern are suppressed as much as possible, and according to the electronic-parts mounting approach of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by having. According to the electronic-parts mounting approach of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented by the anisotropy electric conduction cementing material which could enlarge the electrode according to the above-mentioned configuration, preventing short-circuit of the electrodes which adjoin an electrode in a corner part by having considered as the notching **** configuration in the corner of a point, and was fused becoming what is easy to flow between circuit patterns, and furthermore, having. Furthermore, according to the electronic-parts mounting approach of this invention, the fall of the junction nature of a wiring substrate and electronic parts can be beforehand prevented with the above-mentioned configuration by making a film-like anisotropy electric conduction cementing material follow the component side of a wiring substrate, being able to carry out the temporary adhesion of it certainly, and having it according to the flexibility of the pad in a heat tool.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] (a) It is the important section top view and important section cross-section side elevation in which reaching and showing the electronic unit in connection with this invention in (b).

[Drawing 2] (a) It is the important section top view and important section cross-section side elevation in which reaching and showing the wiring substrate in connection with this invention in (b).

[Drawing 3] The important section top view showing the configuration of the electrode in the wiring substrate in connection with this invention.
[Drawing 4] (a) It is the important section top view in which reaching and showing other examples of the configuration of the electrode in the wiring substrate in connection with this invention in (b).
[Drawing 5] The cross-section side elevation showing notionally the production process of the electronic unit in connection with this invention.
[Drawing 6] The cross-section side elevation showing notionally the production process of the electronic unit in connection with this invention.
[Drawing 7] The cross-section side elevation showing notionally the production process of the electronic unit in connection with this invention.
[Drawing 8] The cross-section side elevation showing notionally the production process of the electronic unit in connection with this invention.
[Drawing 9] The important section cross-section side elevation showing the conventional electronic unit.
[Drawing 10] The important section top view showing the conventional wiring substrate.
[Drawing 11] (a) It is the conceptual diagram in which is attained to and (b) shows the production process of the conventional electronic unit.
[Description of Notations]
1 — Electronic unit
10 — Wiring substrate,
11 — Surface circuit pattern,
11A — Electrode,
12 — Insulating layer,
15 — Solder resist,
15a — Opening,
20 — Raise in basic wages IC chip (electronic parts),
30 — Anisotropy electric conduction cementing material,
40 — Heat tool,
41 — Pad.

[Translation done.]